Letters

X3D: Heterogeneous Monolithic 3D Integration of "X" (Arbitrary) Nanowires: Silicon, III–V, and Carbon Nanotubes

Pritpal S. Kanhaiya, Yosi Stein, Wenjie Lu, Jesús A. del Alamo, and Max M. Shulaker

***Abstract*—We experimentally demonstrate a new paradigm for monolithic three-dimensional (3D) integration: X3D, which enables a wide range of semiconductors – including silicon (Si), III–V, and nanotechnologies such as carbon nanotubes (CNTs) – to be heterogeneously integrated together in monolithic 3D integrated systems. Such flexible heterogeneous integration has potential for a wide range of applications, as each layer of monolithic X3D integrated circuits (ICs) can be customized for specific functionality (e.g., wide-bandgap III–V-based circuits for power management, CNT field-effect transistors (CNFETs) for energy-efficient computing, and tailored materials for custom sensors or imagers). As a case study, we experimentally demonstrate monolithic X3D ICs with five vertical circuit layers heterogeneously integrating three different semiconductors: Si junctionless nanowire field-effect transistors (JNFETs), III–V JNFETs, and CNFETs (also junctionless). The layers of monolithic X3D IC are, from bottom-to-top: Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III–V n-JNFETs. Each layer is fabricated using an identical process flow for ease of integration. Importantly, we show that circuits fabricated on each vertical layer are agnostic to subsequent monolithic X3D processing, experimentally demonstrating ability to interleave these "X" (arbitrary) semiconductors in arbitrary vertical ordering. As a final demonstration, we fabricate complementary digital logic circuits comprising different technologies that span multiple vertical circuit layers. This work demonstrates a new paradigm for ICs, allowing for flexible and customizable electronic systems.**

***Index Terms*—Monolithic 3D, junctionless transistors, heterogeneous integration, nanowires.**

I. Introduction

As CONTINUED physical and equivalent scaling (e.g., Dennard scaling [1]) of silicon-based field-effect transistors (FETs) yields diminishing returns [2], multiple alternative paths for improving the energy efficiency of digital very-large-scale-integrated (VLSI) circuits and systems are being pursued.

Manuscript received October 16, 2018; revised January 3, 2019; accepted February 18, 2019. Date of publication March 5, 2019; date of current version March 14, 2019. This work was supported in part by Analog Devices Inc., (ADI), in part by NSF under Grant CNS-1657303, and in part by DARPA under Grant W909MY-16-0001. The review of this letter was arranged by associate editor Jian-Jang Huang. *(Corresponding author: Pritpal Singh Kanhaiya.)*

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Digital Object Identifier 10.1109/TNANO.2019.2902114

On one hand, improved FETs fabricated with beyond-silicon technologies ranging from III–V compound semiconductors to emerging nanotechnologies such as carbon nanotubes (CNTs) promise improved scalability and energy efficiency. For instance, digital systems fabricated from CNT FETs (CNFETs) versus silicon FETs promise a 10× improvement in energy-delay product (EDP: a metric of energy efficiency) [3]–[6].

On the other hand, new integration techniques, such as three-dimensional (3D) integrated circuits (ICs), promise new computing architectures and further energy efficiency benefits. Monolithic 3D integration, whereby multiple layers of circuits are fabricated directly over one-another on the same starting substrate (i.e., no wafer bonding required), enables nano-scale inter-layer vias (ILVs) to connect vertical layers of a 3D IC providing fine-grained and dense vertical connectivity between circuit layers [7], [8]. Such massive physical connectivity can translate to large increases in data bandwidth between vertical layers, which can improve energy efficiency by >100× for abundant-data applications [9], [10].

Despite these promising directions, there are substantial challenges for realizing these future electronic systems. For instance, monolithic 3D integration requires that all processing on the upper layers must be low temperature (e.g., <400 °C), as higher temperatures damage lower-level FETs and destroy low-temperature back-end-of-line (BEOL) metal interconnects [10]. As a result, many technologies, including silicon and beyond-silicon semiconductors (such as III–V compound semiconductors), are challenging to integrate in monolithic 3D systems, since they require high-temperature processing for both high-quality single-crystalline synthesis and high-temperature anneals (>1000 °C) for doping and junction formation in traditional FETs.

Here, we present a new paradigm for electronic systems: X3D. X3D enables a wide-range of semiconductors, including conventional silicon, next-generation III–V compounds (as an example, in this work we use GaAs), and nanotechnologies such as CNTs to be heterogeneously integrated over the same starting substrate in a monolithic 3D IC. Thus, X3D combines the energy efficiency benefits of beyond-silicon devices, the benefits of monolithic 3D integration, and the flexibility of customizing different vertical 3D layers enabled by a wide-range of semiconductors. Importantly, this work is in stark contrast to previous demonstrations of monolithic 3D integration of heterogeneous

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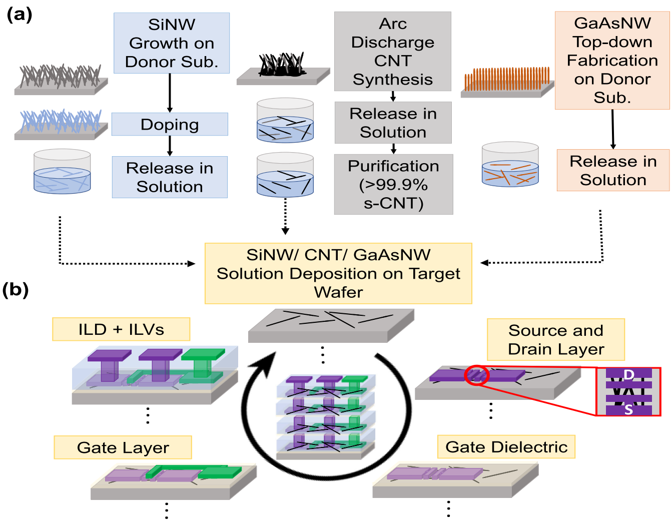

Fig. 1. Process flow of X3D. (a) Schematic of NW and CNT synthesis and doping. (Left) SiNWs are synthesized and gas-phased doped post-synthesis on a donor substrate. Ultrasonication releases the SiNWs in IPA. (Middle) CNTs are grown via arc discharge, released in solution and sorted via density gradient centrifugation. (Right) GaAsNWs are synthesized through a top-down fabrication of a pre-doped GaAs substrate. Ultrasonication releases the GaAsNWs in IPA. (b) VLSI–scalable and CMOS compatible device fabrication flow of each X3D vertical layer. The “X” semiconductor solution is deposited, followed by PVD of source, drain, and gate (Ti/Pt) with ALD-deposited HfO_X as the high-k gate dielectric. Between each vertical layer, an inter-layer dielectric (PVD SiO_2) is deposited and ILVs (metal vias) are defined. These same steps are repeated for every layer in the X3D chip.

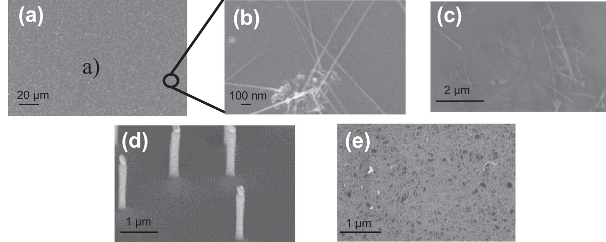

Fig. 2. SEMs of donor and target substrates. (a–b) single-crystalline SiNWs on donor. (c) SiNWs deposited over the target X3D substrate. (d) GaAsNWs on donor. GaAsNWs are etched by ICP-RIE into an n-doped GaAs substrate. (e) CNTs deposited over the target X3D substrate.

technologies (silicon and CNTs [8], [10]), as upper-layers of circuits were all constrained to CNTs; X3D enables arbitrary vertical interleaving of Si, III–Vs, CNTs, *etc.*

The key to X3D is using junctionless nanowire FETs (JNFETs) [11] in which: (1) the high temperature synthesis and uniform doping of each “X” semiconducting channel is performed on a donor substrate (i.e., which is separate from the substrate used for circuit fabrication), (2) the “X” nanowires (NWs, including CNTs and Si-/III–V-based NWs) are released in different solutions, and (3) for any circuit layer in the monolithic X3D IC, “X” NWs are deposited on the substrate using a low-temperature process (e.g., solution-based processing), followed by transistor fabrication (all <200 °C). Importantly, there are no additional high-temperature processing steps (e.g., doping) on the target substrate (X3D IC).

II. X3D Process Flow

The process flow for X3D decouples the nanowires’ high-temperature synthesis, doping, and annealing fabrication steps from the low-temperature FET fabrication steps (see Fig. 1). First, NW synthesis of “X” technology is performed on a donor substrate. NWs are then uniformly-doped either by introducing the dopants during NW synthesis (in-situ doping) or post-synthesis (through gas-phase doping or implantation). Following these high-temperature processing steps – which are all performed on the donor substrate (i.e., not on the monolithic X3D IC) – the NWs are released into solution using ultrasonication. To fabricate an “X” layer within a monolithic X3D IC, the desired NW solution is deposited on the target substrate. This solution processing is performed at room-temperature. For FET fabrication, the source, drain, and gate are lithographically patterned, and all NW segments outside FET channel regions are etched away and thus are removed from the circuit. Due to the decoupled NW synthesis and lack of junction formation once on the monolithic X3D IC, all processing on the monolithic X3D IC is <200 °C, rendering the process monolithic 3D compatible as well as silicon CMOS compatible. Following fabrication of each monolithic X3D layer, inter-layer dielectrics (ILDs) are deposited, and ILVs used for metal routing are defined. Importantly, these ILVs can be >1,000× denser versus through-silicon vias (TSVs) owing to monolithic 3D integration, providing dense connectivity between vertical layers of the monolithic X3D IC [7], [8].

The use of NWs is essential, as it allows each of the “X” semiconductors to be released in solution for subsequent use in identical processing steps. JNFETs are essential as the entire NW can be uniformly doped; this enables the NWs to be placed in arbitrary locations across the substrate without requiring specific doping regions or precise alignment with the subsequent transistor formation (e.g., NPN aligning with source, gate, and drain). Moreover, the NWs and JNFETs are ideal pairings as the ultra-thin body thickness of the NWs are essential for JNFET electrostatic control [11], [12].

The detailed NW synthesis flow is shown in Fig. 2. SiNWs are grown in a low-pressure chemical vapor deposition (LPCVD) system via a vapor-liquid-solid (VLS) method [13]. CNTs are synthesized through arc discharge [14], and >99.9% semiconducting CNTs are sorted and released in solution via density gradient centrifugation [15], [16]. GaAsNWs are defined through top-down fabrication using precision reactive ion etching [17], [18]. To form either p-type or n-type JNFETs, the NWs are doped either before or during synthesis (e.g., GaAsNWs are defined in pre-doped GaAs substrate), through gas-phase doping post-synthesis (for SiNWs) [19], [20], or through field-effect doping (for CNTs) [21]–[23]. Post-doping, the NWs are deposited on the target layer of the monolithic X3D through solvent deposition. To do so, the NWs are dispersed in solvent (SiNWs and GaAsNWs in IPA, CNTs in toluene) through ultrasonication. The solution with suspended NWs is then drop-casted and dried on the monolithic X3D IC, depositing the NWs. While we leverage a simple drop-casting technique to deposit the NWs

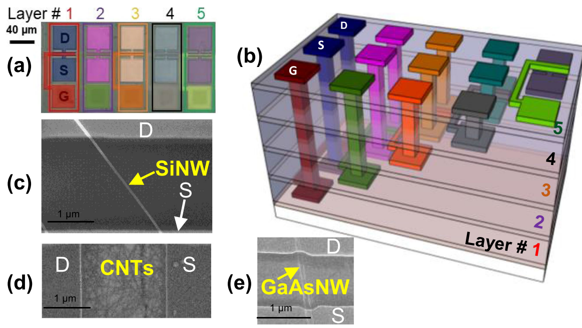

Fig. 3. (a) Optical microscopy image of devices fabricated on each layer of the 5-layer X3D chip, with their respective source, drain, and gate metals highlighted. (b) 3D schematic of fabricated 5-layer X3D stack. SEMs of (c) SiNWs (d ~ 20 nm), (d) CNTs (d ~ 1 nm), and (e) GaAsNWs (d ~ 100 nm) bridging the source and drain contacts. All FETs are fabricated with a top-gate geometry, except for the p-CNFETs (layer 4) which use a local bottom-gate geometry. All FETs have 40 nm source and drain contacts (Pt), leverage a high-k metal gate stack (25 nm high-k HfO_X gate dielectric, 20 nm Pt gate). The inter-layer dielectrics (ILDs) are all 100 nm SiO_2.

over the monolithic X3D IC for ease of integration, a range of techniques have demonstrated aligned and dense NW deposition from solution [24]–[28]. Once the doped NWs are deposited on the substrate, the JNFETs to form the circuit on that layer of the monolithic X3D IC are defined. The source, gate, and drain (~1 nm titanium /~30 nm platinum) are lithographically patterned, while the high-k gate dielectric (~25 nm HfO_x) is ALD-deposited (all processing <200 °C).

III. Experimental Results

As an experimental demonstration of X3D, we fabricate a monolithic X3D IC with 5 vertical circuit layers comprising 3 different semiconductors (Si, III–V, and CNTs). As shown in Fig. 3, it comprises (from bottom to top): Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III–V n-JNFETs. The ordering of the layers is chosen to explicitly demonstrate the ability to arbitrarily stack these technologies within the monolithic X3D IC: silicon (layer 3) is integrated over silicon (layer 1), CNT (layer 4) is integrated over CNT (layer 2), CNT (layer 2) is integrated over silicon (layer 1), silicon (layer 3) is integrated over CNT (layer 2), and III–V is integrated over both silicon (layers 1 and 3) and CNT (layers 2 and 4). The FETs shown in Fig. 3(a) are staggered for visibility; FETs can be vertically overlapping as well. To characterize the monolithic X3D process, we fabricate and measure the JNFETs across every layer of the monolithic X3D IC. To validate that the JNFETs can be vertically interleaved on arbitrary circuit layers, we measure the JNFETs on each layer immediately after fabrication of that layer, as well as after the entire subsequent monolithic X3D processing (see Fig. 4). As shown in Fig. 4(c), the JNFETs on all layers exhibit negligible performance change due to subsequent monolithic X3D processing; the on-state drive current (I_{ON}, i.e., measured drain current when $|V_{GS}| = |V_{DS}| = V_{DD}$) of each vertical layer immediately after fabrication and post subsequent monolithic X3D processing exhibit insignificant change (we fail to reject the null hypothesis that the average I_{ON} are

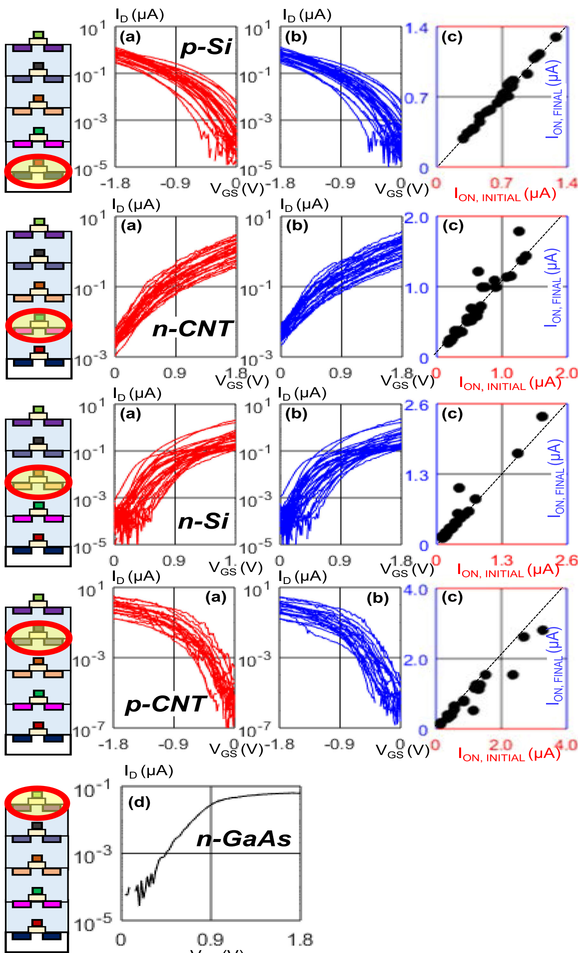

Fig. 4. $I_D - V_{GS}$ characteristics of first four layers of devices (30 FETs per layer). (a) measured immediately after fabrication, and (b) measured again after monolithic X3D processing. (c) I_{ON} pre- and post- monolithic X3D processing shows negligible change resulting from X3D processing. The line with slope of 1 is the ideal case. Sub-threshold slopes ~100–200 mV/decade. (d) $I_D - V_{GS}$ characteristic of a typical GaAs n-JNFET on the fifth layer of the monolithic X3D IC. Post- monolithic X3D processing I_D-V_{GS} are not shown as this is the final layer of the monolithic X3D stack. Si- and GaAs-based JNFETs have ~1–2 NWs per JNFET, while CNT-based JNFETs have ~30 CNTs/µm.

the same before and after monolithic X3D fabrication, using the two samples t-test for difference in mean with 95% confidence [29]).

As a demonstration, we experimentally show functional complementary digital logic circuits spanning multiple vertical circuit layers and semiconductor technologies: between Si p-JNFETs (layer 1) and n-CNFETs (layer 2), and between p-CNFETs (layer 4) and Si n-JNFETs (layer 3) (see Fig. 5). As shown in Fig. 5(a), the source terminals of layers 1 and 2 are connected using ILVs to define the output terminal for inverter 1, and the gate terminals of layers 1 and 2 are likewise connected through ILVs to define the input terminal. The same case holds for inverter 2 spanning layers 3 and 4. Correct inverter logic functionality is illustrated in Fig. 5(c) when operating at a supply voltage of 1.8 V_{DD}, where logical low input signals return a logical high output and logical high input signals return a logical low output.

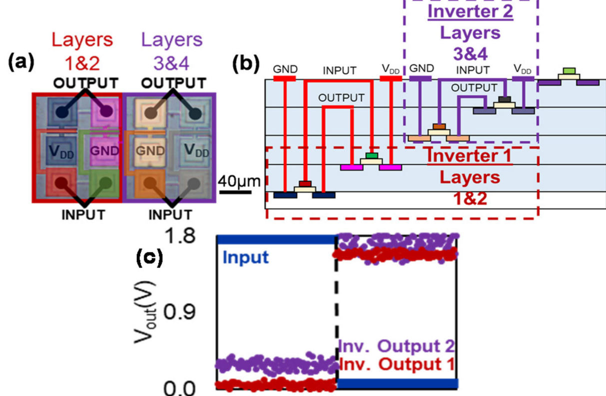

Fig. 5. (a) Optical microscopy image of two fabricated monolithic X3D CMOS inverters, with inverter 1 spanning layer 1 (Si p-JNFET) and layer 2 (n-CNFET), and inverter 2 spanning layer 3 (Si n-JNFET) and layer 4 (p-CNFET). (b) Cross-sectional schematic of monolithic X3D inverters. (c) Output voltages given inputs toggled between 0 V and V_{DD} (1.8 V).

IV. Conclusion

This work demonstrates X3D, a new paradigm for monolithic 3D integration, which enables heterogeneous integration of a wide range of nanowire-based semiconductors. With our first demonstration of X3D, we integrate three different technologies (silicon, CNTs, and III–Vs) spanning 5 vertically-interleaved layers, forming complementary digital logic. Importantly, X3D provides a framework that allows all layers to be fabricated with identical processing steps for ease-of-integration and allows arbitrary ordering of layers. While an example case-study, such flexible and customizable heterogeneous integration has potential for a wide range of applications. Each layer of monolithic X3D ICs can be customized for specific functionality; e.g., wide-bandgap III–Vs for power management, CNTs for energy efficient computing, and tailored bandgaps for specialized sensors or imagers. Thus, this work provides a new direction for future generations of electronic systems to grow in diversity and customization, integrating an increasingly wide range of new technologies within ICs.

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